WHAT IS CLAIMED IS:

1. A system for maintaining a stable synchronization state in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

a first circuit portion operable to generate a load signal indicative of a known acceptable state from which a cycle may be loaded;

a second circuit portion in communication with said first circuit portion, said second circuit portion operating to generate a lock signal indicative of a tolerable tracked skew between said first clock signal and said second clock signal; and

a third circuit portion, operating responsive to said load signal, said lock signal, and a zero skew point indicator, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal.

2. The system as recited in claim 1, further comprising a synchronizer configuration interface in communication with each of said first circuit portion, said second circuit portion and said third circuit portion, wherein said synchronizer configuration interface is operable to provide a configuration signal indicative of a skew tolerance between said first clock signal and second clock signal.

3. The system as recited in claim 1, further comprising a synchronizer configuration interface in communication with each of said first circuit portion, said second circuit portion and said third circuit portion, wherein said synchronizer configuration interface is operable to provide a configuration signal indicative of a latency value with respect to at least one of said first clock signal and said second clock signal.

4. The system as recited in claim 1, wherein said first circuit portion comprises a cycle and sequence generator.

5. The system as recited in claim 1, wherein said first circuit portion generates said load signal in response to a stable state signal (stable_state) generated by said third circuit portion and a synchronous rising edge signal (sync_redge) generated by a synchronizer pulse detector.

6. The system as recited in claim 1, wherein said first circuit portion generates said load signal in response to a stable state signal (stable_state) generated by said third circuit portion, a synchronous rising edge signal (sync_redge) generated by a sync pulse detector, a sampled rising edge signal (syncb0_cr) generated by a sampling block, a sampled falling edge signal (syncb0_cf) signal generated by said sampling block, and phase detection signals (pd_b_cr and pd_b_cf) provided by a phase detector.

7. The system as recited in claim 1, wherein said second circuit portion comprises a skew state detector.

8. The system as recited in claim 1, wherein said lock signal is generated in response to coincident rising edges of said first clock signal and said second clock signal.

9. The system as recited in claim 1, wherein said lock signal is generated in response to a zero sequence state signal (seq_state = Z) provided by a precision sequence detector.

10. The system as recited in claim 1, wherein said third circuit portion comprises a stable state detector.

11. The system as recited in claim 1, wherein said third circuit portion is operable to transmit said synchronization stable state signal to said first circuitry disposed in said first clock domain.

12. The system as recited in claim 1, wherein said lock signal is operable as a zero skew point indicator in a 1:1 ratio mode wherein said N/M =1.

13. The system as recited in claim 1, wherein said third circuit portion provides said zero skew point indicator by ANDing a cycle signal provided by said first circuit portion and a pd_z signal provided by said second circuit portion.

14. A method for maintaining a stable synchronization state in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

generating a load signal indicative of a known acceptable state from which a cycle may be loaded;

generating a lock signal indicative of a tolerable tracked skew between said first clock signal and said second clock signal; and

responsive to said load signal, said lock signal and a zero skew pint indicator, generating a synchronization stable state signal indicative of locking between said first clock signal and said clock signal.

15. The method as recited in claim 14, wherein said load signal is generated in response to a stable state signal (stable_state) and a synchronous rising edge signal (sync_redge).

16. The method as recited in claim 14, wherein said load signal is generated in response to a stable state signal (stable_state) generated by said third circuit portion, a synchronous rising edge signal (sync_redge) generated by a sync pulse detector, a sampled rising edge signal (syncb0_cr) generated by a sampling block, a sampled falling edge signal (syncb0_cf) signal generated by said sampling block, and phase detection signals (pd_b_cr and pd_b_cf) provided by a phase detector.

17. The method as recited in claim 14, wherein said lock signal is generated in response to coincident rising edges of said first clock signal and said second clock signal.

18. The method as recited in claim 14, wherein said lock signal is generated in response to a zero sequence state signal (seq_state = Z) provided by a precision sequence detector.

19. The method as recited in claim 14, wherein said zero skew point indicator is provided by ANDing a cycle signal and a pd_z signal.

20. A computer system having an apparatus for maintaining a stable synchronization state in a programmable clock synchronizer used in effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where N/M $\geq$ 1, comprising:

a cycle and sequence generator operable to generate a load signal indicative of a known acceptable state from which a cycle may be loaded;

a skew state detector in communication with said cycle and sequence generator, said skew state detector operating to generate a lock signal indicative of a tolerable treated skew between said first clock signal and said second clock signal; and

a stable state detector, operating responsive to said load signal, said lock signal and a zero skew point indicator, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal.

21. The computer system as recited in claim 20, wherein said cycle and sequence generator generates said load signal in response to a stable state signal (stable_state) generated by said stable state detector and a synchronous rising edge signal (sync_redge) generated by a synchronizer pulse detector.

22. The computer system as recited in claim 20, wherein said cycle and sequence generator generates said load signal in response to a stable state signal (stable_state) generated by said stable state detector, a synchronous rising edge signal (sync_redge) generated by a sync pulse detector, a sampled rising edge signal (syncb0_cr) generated by a sampling block, a sampled falling edge signal (syncb0_cf) signal generated by said sampling block, and phase detection signals (pd_b_cr and pd_b_cf) provided by a phase detector.

23. The computer system as recited in claim 20, wherein said lock signal is generated in response to coincident rising edges of said first clock signal and said second clock signal.

24. The computer system as recited in claim 20, wherein said lock signal is generated in response to a zero sequence state signal (seq_state = Z) provided by a precision sequence detector.

25. The computer system as recited in claim 20, wherein said stable state detector is operable to transmit said synchronization stable state signal to said first circuitry disposed in said first clock domain.

26. The method as recited in claim 20, wherein said zero skew point indicator is provided by ANDing a cycle signal and a pd_z signal.